Precision, 500 ns Settling BiFET Op Amp

AD744

FEATURES

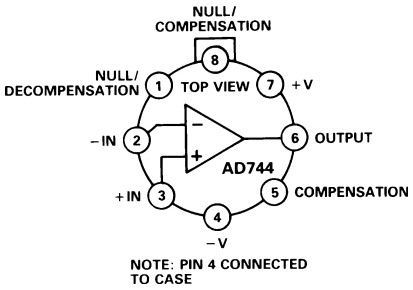
AC PERFORMANCE
- 500 ns Settling to 0.01% for 10 V Step
- 1.5 μs Settling to 0.0025% for 10 V Step
- 75 V/μs Slew Rate
- 0.0003% Total Harmonic Distortion (THD)
- 13 MHz Gain Bandwidth – Internal Compensation
- >200 MHz Gain Bandwidth (G = 1000) External Decompensation
- >1000 pF Capacitive Load Drive Capability with 10 V/μs Slew Rate – External Compensation

DC PERFORMANCE
- 0.5 mV max Offset Voltage (AD744B)
- 10 μV/°C max Drift (AD744B)
- 250 V/mV min Open-Loop Gain (AD744B)
- Available in Plastic Mini-DIP, Plastic SOIC, Hermetic Cerdip, Hermetic Metal Can Packages and Chip Form
- Surface Mount (SOIC) Package Available in Tape and Reel in Accordance with EIA-481A Standard

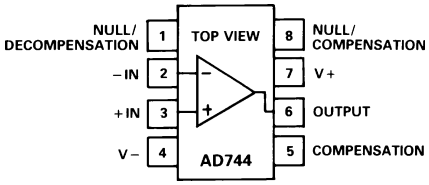
APPLICATIONS
- Output Buffers for 12-Bit, 14-Bit and 16-Bit DACs, ADC Buffers, Cable Drivers, Wideband Preamplifiers and Active Filters

CONNECTION DIAGRAMS

TO-99 (H) Package



8-Lead Plastic Mini-DIP (N)
8-Lead SOIC (R) Package and
8-Lead Cerdip (Q) Packages



PRODUCT DESCRIPTION

The AD744 is a fast-settling, precision, FET input, monolithic operational amplifier. It offers the excellent dc characteristics of the AD711 BiFET family with enhanced settling, slew rate, and bandwidth. The AD744 also offers the option of using custom compensation to achieve exceptional capacitive load drive capability.

The single-pole response of the AD744 provides fast settling: 500 ns to 0.01%. This feature, combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12-bit, 14-bit or 16-bit DACs and ADCs. Furthermore, the AD744's low total harmonic distortion (THD) level of 0.0003% and gain bandwidth product of 13 MHz make it an ideal amplifier for demanding audio applications. It is also an excellent choice for use in active filters in 12-bit, 14-bit and 16-bit data acquisition systems.

The AD744 is internally compensated for stable operation as a unity gain inverter or as a noninverting amplifier with a gain of two or greater. External compensation may be applied to the AD744 for stable operation as a unity gain follower. External compensation also allows the AD744 to drive 1000 pF capacitive loads, slewing at 10 V/μs with full stability.

Alternatively, external decompensation may be used to increase the gain bandwidth of the AD744 to over 200 MHz at high gains. This makes the AD744 ideal for use as ac preamps in digital signal processing (DSP) front ends.

The AD744 is available in five performance grades. The AD744J and AD744K are rated over the commercial temperature range of 0°C to +70°C. The AD744A and AD744B are rated over the industrial temperature range of –40°C to +85°C. The AD744T is rated over the military temperature range of –55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD744 is available in an 8-lead plastic mini-DIP, 8-lead small outline, 8-lead cerdip or TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD744 is a high-speed BiFET op amp that offers excellent performance at competitive prices. It outperforms the OPA602/OPA606, LF356 and LF400.
2. The AD744 offers exceptional dynamic response. It settles to 0.01% in 500 ns and has a 100% tested minimum slew rate of 50 V/μs (AD744B).
3. The combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ionimplanted JFETs provide outstanding dc precision. Input offset voltage, input bias current, and input offset current are specified in the warmed-up condition; all are 100% tested.

AD744—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD744J/A/S Min	AD744J/A/S Typ	AD744J/A/S Max	AD744K/B/T Min	AD744K/B/T Typ	AD744K/B/T Max	Unit
INPUT OFFSET VOLTAGE[1]								
Initial Offset			0.3	1.0		0.25	0.5	mV
Offset	T_{MIN} to T_{MAX}			2			1.0	mV
vs. Temp.			5	20		5	10	µV/°C
vs. Supply[2]		82	95		88	100		dB
vs. Supply	T_{MIN} to T_{MAX}	82			88			dB
Long-Term Stability			15			15		µV/month
INPUT BIAS CURRENT[3]								
Either Input	V_{CM} = 0 V		30	100		30	100	pA
Either Input @ T_{MAX} =	V_{CM} = 0 V							
J, K	70°C		0.7	2.3		0.7	2.3	nA
A, B, C	85°C		1.9	6.4		1.9	6.4	nA
S, T	125°C		31	102		31	102	nA
Either Input	V_{CM} = +10 V		40	150		40	150	pA
Offset Current	V_{CM} = 0 V		20	50		10	50	pA
Offset Current @ T_{MAX} =	V_{CM} = 0 V							
J, K	70°C		0.4	1.1		0.2	1.1	nA
A, B, C	85°C		1.3	3.2		0.6	3.2	nA
S, T	125°C		20	52		10	52	nA
FREQUENCY RESPONSE								
Gain BW, Small Signal	G = –1	8	13		9	13		MHz
Full Power Response	V_O = 20 V p-p		1.2			1.2		MHz
Slew Rate, Unity Gain	G = –1	45	75		50	75		V/µs
Settling Time to 0.01%[4]	G = –1		0.5	0.75		0.5	0.75	µs
Total Harmonic	f = 1 kHz							
Distortion	R1 ≥ 2 kΩ							
	V_O = 3 V rms		0.0003			0.0003		%
INPUT IMPEDANCE								
Differential			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
Common Mode			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
INPUT VOLTAGE RANGE								
Differential[5]			±20			±20		V
Common-Mode Voltage			+14.5, –11.5			+14.5, –11.5		V
Over Max Operating Range[6]		–11		+13	–11		+13	V
Common-Mode								
Rejection Ratio	V_{CM} = ±10 V	78	88		82	88		dB
	T_{MIN} to T_{MAX}	76	84		80	84		dB
	V_{CM} = ±11 V	72	84		78	84		dB
	T_{MIN} to T_{MAX}	70	80		74	80		dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		2			2		µV p-p
	f = 10 Hz		45			45		$nV/\sqrt{Hz}$
	f = 100 Hz		22			22		$nV/\sqrt{Hz}$
	f = 1 kHz		18			18		$nV/\sqrt{Hz}$
	f = 10 kHz		16			16		$nV/\sqrt{Hz}$
INPUT CURRENT NOISE	f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$
OPEN LOOP GAIN[7]	V_O = ±10 V							
	R_{LOAD} ≥ 2 kΩ	200	400		250	400		V/mV
	T_{MIN} to T_{MAX}	100			100			V/mV
OUTPUT CHARACTERISTICS								
Voltage	R_{LOAD} ≥ 2 kΩ	+13, –12.5	+13.9, –13.3		+13, –12.5	+13.9, –13.3		V
	T_{MIN} to T_{MAX}	±12	+13.8, –13.1		±12	+13.8, –13.1		V
Current	Short Circuit		25			25		mA
Capacitive Load[8]	Gain = –1			1000			1000	pF
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±4.5		±18	±4.5		±18	V
Quiescent Current			3.5	5.0		3.5	4.0	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]PSRR test conditions: $+V_S$ = 15 V, $-V_S$ = –12 V to –18 V and $+V_S$ = +12 V to +18 V, $-V_S$ = –15 V.

[3]Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[4]Gain = –1, R_L = 2 k, C_L = 10 pF, refer to Figure 25.

[5]Defined as voltage between inputs, such that neither exceeds ±10 V from ground.

[6]Typically exceeding –14.1 V negative common-mode voltage on either input results in an output phase reversal.

[7]Open-Loop Gain is specified with V_{OS} both nulled and unnulled.

[8]Capacitive load drive specified for C_{COMP} = 20 pF with the device connected as shown in Figure 32. Under these conditions, slew rate = 14 V/µs and 0.01% settling time = 1.5 µs typical. Refer to Table II for optimum compensation while driving a capacitive load.

Specifications subject to change without notice. All min and max specifications are guaranteed.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 500 mW
Input Voltage[3] . . . . . ±18 V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q, H) . . . . . –65°C to +150°C
Storage Temperature Range (N, R) . . . . . –65°C to +125°C
Operating Temperature Range
AD744J/K . . . . . 0°C to +70°C
AD744A/B . . . . . –40°C to +85°C
AD744S/T . . . . . –55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . . . . 300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics
8-Lead Plastic Package: θ_{JA} = 100°C/Watt, θ_{JC} = 33°C/Watt
8-Lead Cerdip Package: θ_{JA} = 110°C/Watt, θ_{JC} = 22°C/Watt
8-Lead Metal Can Package: θ_{JA} = 150°C/Watt, θ_{JC} = 65°C/Watt
8-Lead SOIC Package: θ_{JA} = 160°C/Watt, θ_{JC} = 42°C/Watt

[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

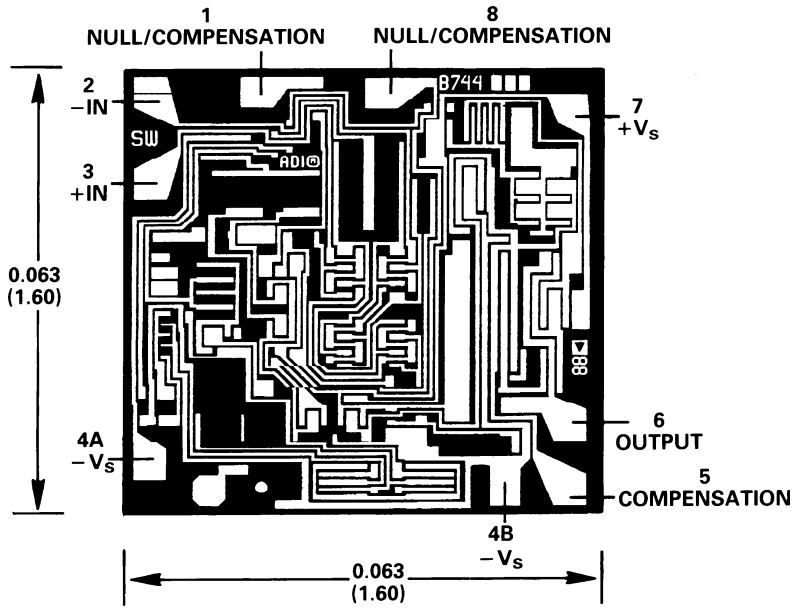
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD744JN	0°C to +70°C	N-8
AD744KN	0°C to +70°C	N-8
AD744JR	0°C to +70°C	SO-8
AD744KR	0°C to +70°C	SO-8
AD744AQ	–40°C to +85°C	Q-8
AD744BQ	–40°C to +85°C	Q-8
AD744AH	–40°C to +85°C	H-08A
AD744JCHIPS	0°C to +70°C	Die
AD744JR-REEL	0°C to +70°C	Tape/Reel 13"
AD744JR-REEL 7	0°C to +70°C	Tape/Reel 7"
AD744KR-REEL	0°C to +70°C	Tape/Reel 13"
AD744KR-REEL 7	0°C to +70°C	Tape/Reel 7"
AD744TA/883B	–55°C to +125°C	H-08

*N = Plastic DIP; SO = Small Outline IC; Q = Cerdip; H = TO-99 Metal Can.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



In either case, the capacitance C_X causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op amp's output. If the value of C_X can be estimated with reasonable accuracy, Equation 2 can be used to choose the correct value for a small capacitor, C_L, which will optimize amplifier response. If the value of C_X is not known, C_L should be a variable capacitor.

As an aid to the designer, the optimum value of C_L for one specific amplifier connection can be determined from the graph of Figure 41. This graph has been produced for the case where the AD744 is connected as in Figures 39 and 40 with a practical minimum value for C_{STRAY} of 2 pF and a total C_X value of 7.5 pF.

The approximate value of C_L can be determined for almost any application by solving Equation 2. For example, the AD565/AD744 circuit of Figure 34 constrains all the variables of Equation 2 (G_N = 3.25, R = 10 kΩ, F_O = 13 MHz, and C_X = 32.5 pF) Therefore, under these conditions, C_L= 10.5 pF.

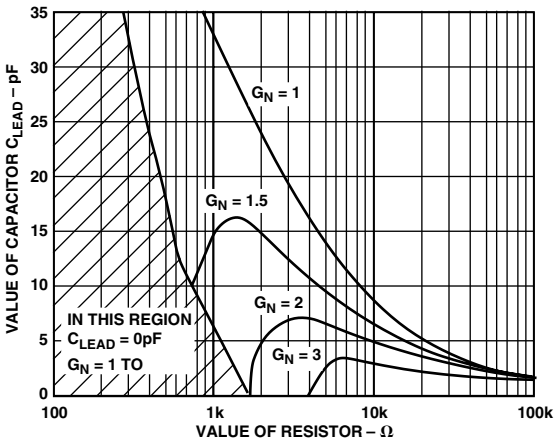


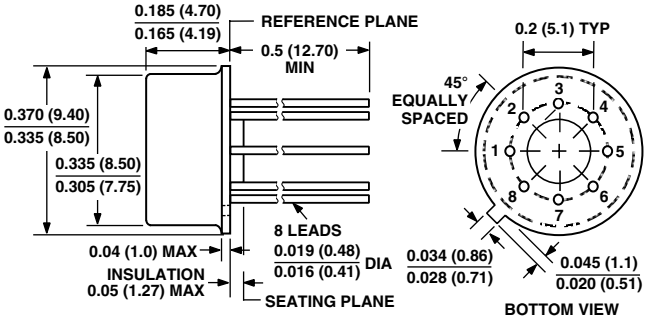
Figure 41. Practical Values of C_L vs. Resistance of R for Various Amplifier Noise Gains

C00833a-0-7/00 (rev. C)

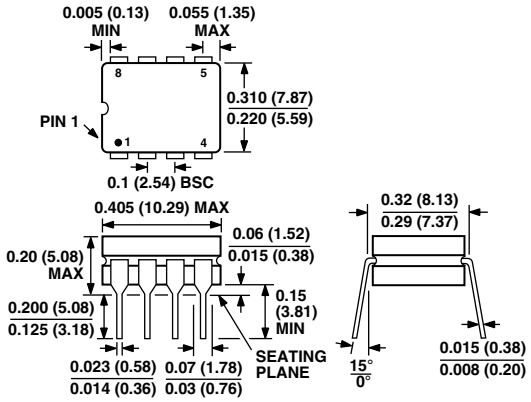
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

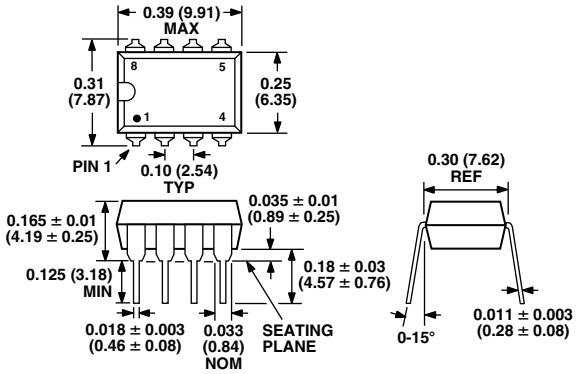
TO-99 (H) Package



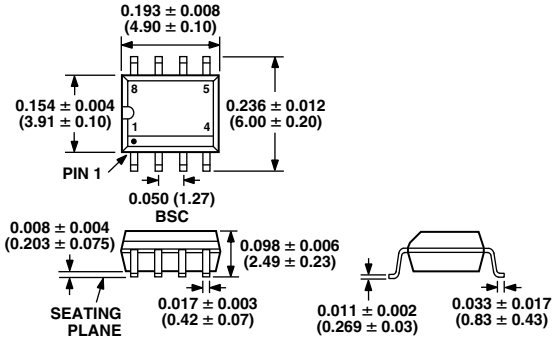
Cerdip (Q) Package



Mini-DIP (N) Package



Small Outline (SO-8) Package



PRINTED IN U.S.A.